

(U.S. Patent No. 6,322,849) and *Van Buskirk, et al* (U.S. Patent No. 6,316,797). Claims 12-16, 23, and 24 were similarly rejected over AAPA, *Evans, Joshi, and Van Buskirk*. Claims 17-20 and 22 were rejected as rendered obvious by AAPA, *Evans, Joshi, and Van Buskirk* in view of *Hayashi* (U.S. Patent 6,362,503) and *Otto, et al* (U.S. Patent No. 6,284,712). These rejections are respectfully traversed. Reconsideration and withdrawal of these rejections are respectfully requested in view of the above amendments and the remarks which follow.

Claim 18 is now cancelled, claims 1, 12, and 19-21 have been amended, and new claims 27-31 have been added to more properly claim the subject matter of the invention. No new matter for the current amendments to the claims has been added. Support for the amendments is found in the specification, drawings figures and/or in the previously pending claims.

- A. Claims 1 and 4 are Distinguishable over Applicants Admitted Prior Art and *Evans*, Neither of Which Teach or Suggest a First Anneal Prior to Top Electrode Etching and a Second Anneal After Top Electrode Etching.

As amended, claim 1 recites the following steps:

annealing the layer of ferroelectric dielectric material with a first anneal;

deposition of an electrically conductive top electrode layer;

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer;

annealing the layer of ferroelectric dielectric material with another anneal after etching the electrically conductive top electrode layer.

Claim 4 includes these steps through its dependence on claim 1.

In contrast, in AAPA, furnace annealing is performed prior to testing after forming the top electrode layer. In *Evans*, a second anneal can be performed after the top electrodes 22 are etched. However, there is no teaching or suggestion in either AAPA or *Evans* that a rapid thermal anneal and another anneal are performed both before and after forming the top electrode. Furthermore, performing the second anneal in the atmosphere as

now claimed is also not taught or suggested in these references. Accordingly, claims 1 and 4 are believed patentably distinguishable over AAPA and *Evans*.

B. Claims 2, 3 and 5-11 are Distinguishable over AAPA, *Evans*, *Joshi* and *Van Buskirk*, None of Which Teach or Suggest a First Anneal Prior to Top Electrode Etching and a Second Anneal After Top Electrode Etching.

Claims 2, 3 and 5-11 each include the above steps of claim 1 through their direct or indirect dependence upon claim 1.

As discussed above, there is no teaching or suggestion in either AAPA or *Evans* that a rapid thermal anneal and another anneal are performed both before and after forming the top electrode. Furthermore, neither *Joshi* nor *Van Buskirk* teach or suggest this method step. Accordingly, claims 2, 3 and 5-11 are also believed patentably distinguishable over AAPA and *Evans*.

C. Claims 12-16, 23 and 24 are Distinguishable over AAPA, *Evans*, *Joshi* and *Van Buskirk* as also Requiring a First Anneal Prior to Top Electrode Etching and a Second Anneal After Top Electrode Etching.

Independent claim 12 includes the following steps:

annealing the layer of ferroelectric dielectric material with a first anneal;

deposition of an electrically conductive top electrode layer comprising a noble metal oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed in an environment comprising a mixture of oxygen and inert gas, the oxygen having partial pressure of less than five percent of one atmosphere and performed after the step of deposition of an electrically conductive top electrode layer.

Claims 13-16, 23 and 24 each also include the recited method steps through their dependence on claim 12. Accordingly, and as discussed above, because there is no teaching or suggestion in any of AAPA, *Evans*, *Joshi* or *Van Buskirk* that a rapid thermal anneal and another anneal are performed both before and after forming the top electrode, claims 12-16, 23 and 24 are also believed patentably distinguishable over these references.

- D. Claims 17-20 and 22 are Distinguishable over AAPA, Evans, Joshi, Van Buskirk, Hayashi and Otto as also Requiring a First Anneal Prior to Top Electrode Etching and a Second Anneal After Top Electrode Etching.

Claims 17-20 and 22 each also include the method step of amended claim 12 discussed above in connection with claim 12. Neither *Hayashi* nor *Otto* teach or suggest that a rapid thermal anneal and another anneal are performed both before and after forming the top electrode. Accordingly, claims 17-20 and 22 are also patentably distinguishable over AAPA, *Evans*, *Joshi*, *Van Buskirk*, *Hayashi* and *Otto*.

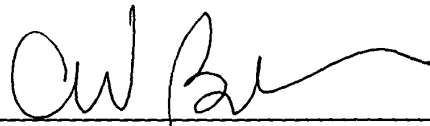
E. Conclusion.

Newly presented claims 27-31 include the distinguishing features of the pending claims discussed above.

Applicant hereby petitions for a 2-month extension, to extend the 3-month shortened statutory period for response from July 10, 2002, to September 10, 2002. The \$574 check enclosed herewith includes \$400 which represents the large entity 2-month extension fee. The enclosed check also includes \$84 representing 1 new independent claims over 3 and \$90 for 5 new total claims over 20. Please charge Deposit Account 50-1123 any fee deficiency associated with this transmittal.

Should any issues remain, the Examiner is kindly asked to the telephone the undersigned.

Respectfully submitted,



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MARKED UP COPY OF AMENDED CLAIMS

1. (Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:
deposition of an electrically conductive bottom electrode layer;
deposition of a layer of ferroelectric dielectric material;
annealing the layer of ferroelectric dielectric material with a first anneal;
deposition of an electrically conductive top electrode layer; [and]
annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer;
etching the electrically conductive top electrode layer; and
annealing the layer of ferroelectric dielectric material with another anneal after etching the electrically conductive top electrode layer.

12. (Amended) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:
deposition of an electrically conductive bottom electrode layer comprising a noble metal;
deposition of a layer of ferroelectric dielectric material;
annealing the layer of ferroelectric dielectric material with a first anneal;
deposition of an electrically conductive top electrode layer comprising a noble metal oxide; and
annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed in an environment comprising a mixture of oxygen and inert gas, the oxygen having partial pressure of less than five percent of one atmosphere [by rapid thermal annealing] and performed after the step of deposition of an electrically conductive top electrode layer.

19. (Amended) The process of Claim 12 [18] wherein the second anneal is performed in an environment comprising oxygen at a partial pressure of approximately one percent.

20. (Amended) The process of Claim 12 [18] wherein the first anneal is performed in an environment comprising a mixture of oxygen and inert gas.

21. (Amended) The process of Claim 12 [18], further comprising the step of:
depositing an encapsulation layer; and
wherein the second anneal is performed after the step of depositing an encapsulation layer.